Claims

1. A control signal generating circuit for an automatic frequency control (AFC) circuit, the control signal generating circuit comprising:

an input for coupling to a tracking circuit of the AFC circuit to receive a digital timing control signal therefrom;

a processor for receiving the digital timing control signal and producing a frequency control signal; and

an output for coupling to a variable frequency generator of the AFC circuit to provide the frequency control signal thereto, the frequency control signal for determining output frequency of the variable frequency generator.

2. A control signal generating circuit in accordance with claim 1, wherein the processor comprises an amplifier coupled to receive the digital timing control signal and a predetermined amplification factor, the amplifier for amplifying the digital timing control signal by the predetermined amplification factor to produce an amplified digital timing control signal, and the amplifier having an output coupled to provide the amplified digital timing control signal.

3. A control signal generating circuit in accordance with claim 2 wherein the processor further comprises an integrator having an input coupled to receive the amplified digital timing control signal, the integrator for integrating the amplified digital timing control signal to produce the frequency control signal, and the integrator having an output coupled to provide the frequency control signal.

4. A control signal generating circuit in accordance with claim 2, wherein the amplifier comprises a multiplier, and wherein the predetermined amplification factor comprises a predetermined multiplication factor, the multiplier for multiplying the digital timing

control signal by the predetermined multiplication factor to produce a multiplied digital timing control signal, and wherein the amplified timing control signal comprises the multiplied digital timing control signal.

5. A control signal generating circuit in accordance with claim 3 wherein the input for coupling to the tracking circuit of the AFC circuit is adapted to receive a plurality of digital outputs.

6. A control signal generating circuit in accordance with claim 3 wherein the input for coupling to the tracking circuit of the AFC circuit is adapted to receive at least three digital outputs, wherein the at least three digital outputs represent three different logic states.

7. A control signal generating circuit in accordance with claim 3 wherein the input for coupling to the tracking circuit of the AFC circuit is adapted to receive three digital outputs, wherein a first of the three digital outputs indicates timing delay, wherein a second of the three digital outputs indicates timing advance, and wherein a third of the three digital outputs indicates timing remains unchanged.

8. A method for generating a frequency control signal for an automatic frequency control (AFC) circuit, the method comprising:

a) receiving a digital timing control signal from a tracking circuit of the AFC circuit;

b) processing the digital timing control signal to produce the frequency control signal; and

c) providing the frequency control signal to a variable frequency generator of the AFC circuit, wherein the frequency control signal determines output frequency of the variable frequency generator.

9. A method in accordance with claim 8, wherein (a) comprises receiving a plurality of digital outputs.

10. A method in accordance with claim 8, wherein (a) comprises receiving at least three digital outputs, wherein the at least three digital outputs represent three different logic states.

11. A method in accordance with claim 8, wherein (a) comprises receiving three digital outputs, wherein a first of the three digital outputs indicates timing delay, wherein a second of the three digital outputs indicates timing delay, and wherein a third of the three digital outputs indicates timing remains unchanged.

12. A method in accordance with claim 8, wherein (b) comprises amplifying the digital timing control signal by a predetermined amplification factor to produce an amplified digital timing control signal, and providing the amplified digital timing control signal.

13. A method in accordance with claim 12, wherein (b) comprises multiplying the digital timing control signal by a predetermined multiplication factor to produce a multiplied digital timing control signal, and providing the multiplied digital timing control signal as the amplified digital timing control signal.

14. A method in accordance with claim 12, wherein (b) further comprises integrating the amplified digital timing control signal to produce the frequency control signal, and providing the frequency control signal.

15. A control signal generating circuit for an automatic frequency control (AFC) circuit, the control signal generating circuit comprising:

an input for coupling to a tracking circuit of the AFC circuit to receive a digital timing control signal therefrom;

a controller for receiving the digital timing control signal, and the controller for passing at least a portion of the digital timing control signal;

a processor for receiving the at least the portion of the digital timing control signal and producing a frequency control signal; and

an output for coupling to a variable frequency generator of the AFC circuit to provide the frequency control signal thereto, the frequency control signal for determining output frequency of the variable frequency generator.

16. A control signal generating circuit in accordance with claim 15, wherein the controller comprises an input for receiving the digital timing control signal, a determinator for determining whether a predetermined initial portion of the digital timing control signal has been received, and an output for providing the at least the portion of the digital timing control signal after the initial portion of the digital timing control signal has been received.

17. A control signal generating circuit in accordance with claim 16, wherein the processor comprises an amplifier coupled to receive the at least the portion of the digital timing control signal and a predetermined amplification factor, the amplifier for amplifying the at least the portion of the digital timing control signal by the predetermined amplification factor to produce an amplified digital timing control signal, and the amplifier having an output coupled to provide the amplified digital timing control signal.

18. A control signal generating circuit in accordance with claim 17 wherein the processor further comprises an integrator having an input coupled to receive the amplified digital timing control signal, the

integrator for integrating the amplified digital timing control signal to produce the frequency control signal, and the integrator having an output coupled to provide the frequency control signal.

19. A control signal generating circuit in accordance with claim 17, wherein the amplifier comprises a multiplier, and wherein the predetermined amplification factor comprises a predetermined multiplication factor, the multiplier for multiplying the at least the portion of the digital timing control signal by the predetermined multiplication factor to produce a multiplied digital timing control signal, and wherein the amplified timing control signal comprises the multiplied digital timing control signal.

20. A control signal generating circuit in accordance with claim 18 wherein the input for coupling to the tracking circuit of the AFC circuit is adapted to receive a plurality of digital outputs, wherein the predetermined initial portion of the digital timing control signal comprises a predetermined number of the plurality of digital outputs, and wherein the determinator comprises a counter for counting the predetermined number of digital outputs.

21. A control signal generating circuit in accordance with claim 18 wherein the input for coupling to the tracking circuit of the AFC circuit is adapted to receive at least three digital outputs, wherein the at least three digital outputs represent three different logic states.

22. A control signal generating circuit in accordance with claim 18 wherein the input for coupling to the tracking circuit of the AFC circuit is adapted to receive three digital outputs, wherein a first of the three digital outputs indicates timing delay, wherein a second of the three digital outputs indicates timing delay, and wherein a third of the three digital outputs indicates timing remains unchanged.

23. A method for generating a frequency control signal for an automatic frequency control (AFC) circuit, the method comprising:

a) receiving a digital timing control signal from a tracking circuit of the AFC circuit;

b) passing at least a portion of the digital timing control signal;

c) processing the at least the portion of the digital timing control signal to produce the frequency control signal; and

d) providing the frequency control signal to a variable frequency generator of the AFC circuit, wherein the frequency control signal determines output frequency of the variable frequency generator.

24. A method in accordance with claim 23, wherein (b) comprises determining whether a predetermined initial portion of the digital timing control signal has been received, and providing the at least the portion of the digital timing control signal after the predetermined initial portion of the digital timing control signal has been received.

25. A method in accordance with claim 24, wherein (a) comprises receiving a plurality of digital outputs.

26. A method in accordance with claim 25, wherein the predetermined initial portion of the digital timing control signal comprises a predetermined number of the plurality of digital outputs, and wherein determining the whether the predetermined initial portion of the digital timing control signal has been received comprises counting the predetermined number of the plurality of digital outputs.

27. A method in accordance with claim 23, wherein (a) comprises receiving at least three digital outputs, wherein the at least three digital outputs represent three different logic states.

28. A method in accordance with claim 23, wherein (a) comprises receiving three digital outputs, wherein a first of the three digital outputs indicates timing delay, wherein a second of the three digital outputs indicates timing delay, and wherein a third of the three digital outputs indicates timing remains unchanged.

28. A method in accordance with claim 23, wherein (c) comprises amplifying the at least the portion of the digital timing control signal by a predetermined amplification factor to produce an amplified digital timing control signal, and providing the amplified digital timing control signal.

29. A method in accordance with claim 28, wherein amplifying the at least the portion of the digital timing control signal by a predetermined amplification factor comprises multiplying the at least the portion digital timing control signal by a predetermined multiplication factor to produce a multiplied digital timing control signal, and providing the multiplied digital timing control signal as the amplified digital timing control signal.

30. A method in accordance with claim 28, wherein (c) further comprises integrating the amplified digital timing control signal to produce the frequency control signal, and providing the frequency control signal.